

VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY

VDMR2M16XS54XX2V35 USER MANUAL

Version : A1

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VDIC-MRAM

HIGH-SPEED 3.3V 128K × 16bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1. DESCRIPTION

The VDMR2M16XS54XX2V35 is a 2.097.152-bit high-speed access time, high-density Magnetoresistive Random Access Memory device. Manufactured with VDIC Very Dense SiP technology. It is organized as one independent die of 128K x 16bit wide data interface.

The VDMR2M16XS54XX2V35 offers MRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR2M16XS54XX2V35 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

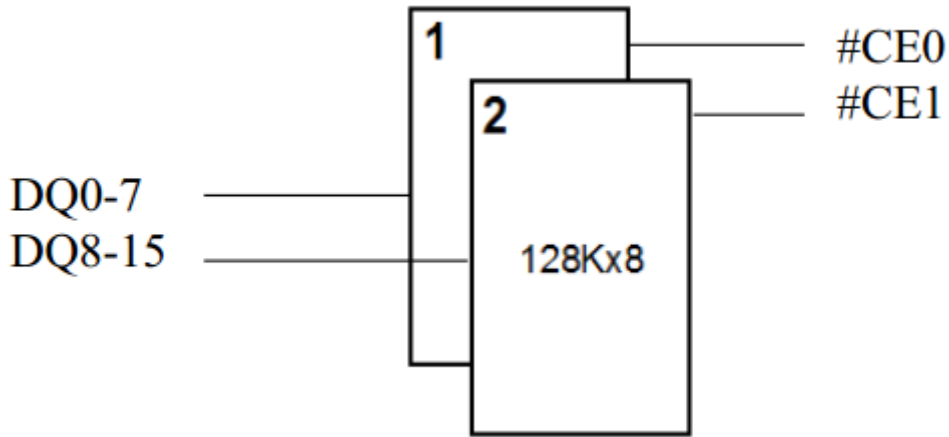
The VDMR2M16XS54XX2V35 has one die. The die can be selected separately with dedicated #CEn. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDMR2M16XS54XX2V35 is available in a 54-pin SOP package.

2. FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at storage temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design
- Stack of two 1Mbit MRAM
- Organized as two die of 128k x 8 bit memory
- Two independent Die Select
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Industrial, Automotive Temperatures
- 54-lead SOP package

3. BLOCK DIAGRAM



(All other signals are common to the memory)

Figure 1 Block diagram

4. PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
DQ9	1	54	DQ14
DQ8	2	53	DQ15
#CE1	3	52	NC
NC	4	51	NC
NC	5	50	NC
A0	6	49	NC
A1	7	48	NC
A2	8	47	NC
A3	9	46	A16
A4	10	45	A15
#CE0	11	44	#OE
DQ0	12	43	DQ7
DQ1	13	42	DQ6
VCC	14	41	VSS
VSS	15	40	VCC
DQ2	16	39	DQ5
DQ3	17	38	DQ4
#WE	18	37	NC
A5	19	36	A14
A6	20	35	A13
A7	21	34	A12
A8	22	33	A11
A9	23	32	A10
NC	24	31	NC
NC	25	30	NC
DQ11	26	29	DQ12
DQ10	27	28	DQ13

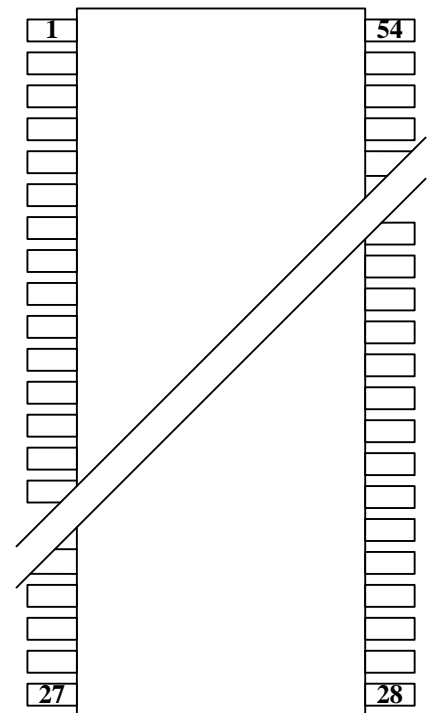


Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CE0,#CE1	Die select	Disables or enables memory die operation
A0 ~ A16	Address	18-bit addresses
#WE	Write enable	Enables write operation common to all memory dies
#OE	Output enable	Enables data output common to all memory dies
DQ0~ DQ15	Data input/output	Data inputs/outputs 16-bit wide bus
V _{CC} /V _{SS}	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	These pins are recommended to be left No Connection on the device.

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than the maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{DD} supply relative to V _{SS}	V _{CC}	-0.5 to +4.0	V
Voltage on any pin relative to V _{SS}	V _{IN}	-0.5 to V _{CC} +0.5	V
Power Dissipation	P _D	1	W
Operating Temperature Range	T _{OPR}	-45~ +95	°C
Storage Temperature Range	T _{STG}	-55 to +150	°C

5.2. RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.2	—	$V_{DD}+0.3$	V
Input low voltage	V_{IL}	-0.5	—	0.8	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 4 DC characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	$I_{OL} = +4mA$	—	0.4	V
Output voltage high level	V_{OH}	$I_{OL} = -4mA$	2.4	—	V

6. TYPICAL APPLICATION

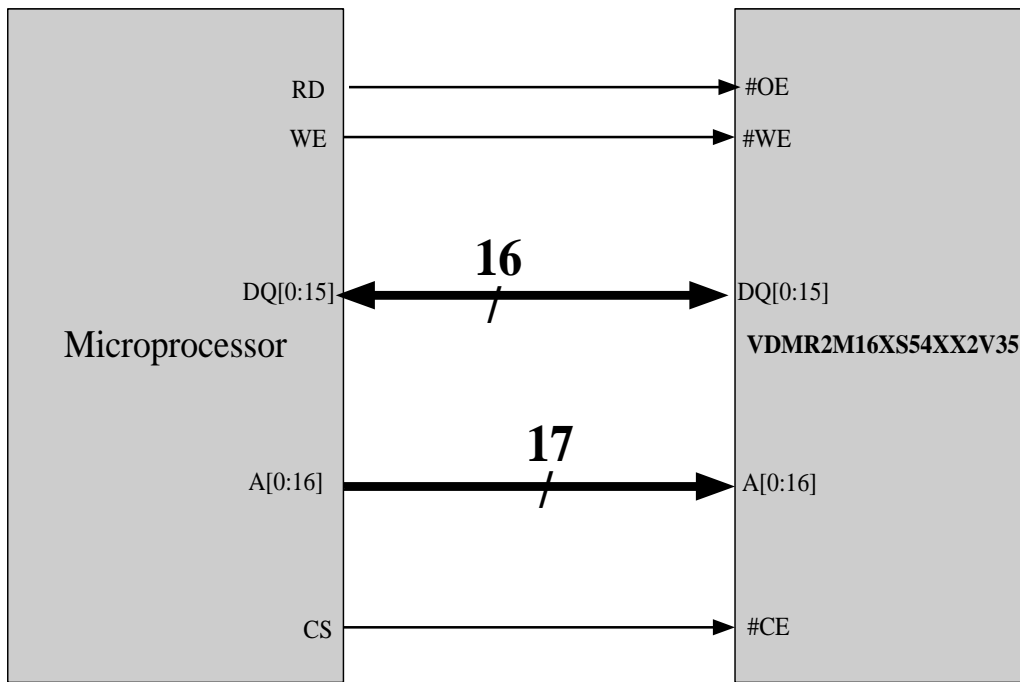


Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>MR</u>	<u>2M</u>	<u>16</u>	<u>V</u>	<u>S</u>	<u>54</u>	<u>E</u>	<u>E</u>	<u>2</u>	<u>V</u>	<u>35</u>	-
VDIC												
MRAM												
Capability: 2M bit												
Bus Width: 16bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: S=SOP												
54=54 Pin												
Temperature::E=0~70°C;I=-40~85°C;S=Specific												
Quality: E= Sample; B= Industry; S= Space												
Stacking Layer:2=2layer												
Power Supply :V=3.3V												
Speed:35= 35ns												
-I、 -K or blank space=First Version												

table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDMR2M16VS54EE2V35	2M	16	-	-	-	SOP54	0 ~ + 70
VDMR2M16VS54IB2V35	2M	16	-	-	-	SOP54	-40 ~ + 85
VDMR2M16RS54SS2V35	2M	16	>60	<40	>37	SOP54	-45 ~ + 95

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8. PACKAGE DIMENSIONS

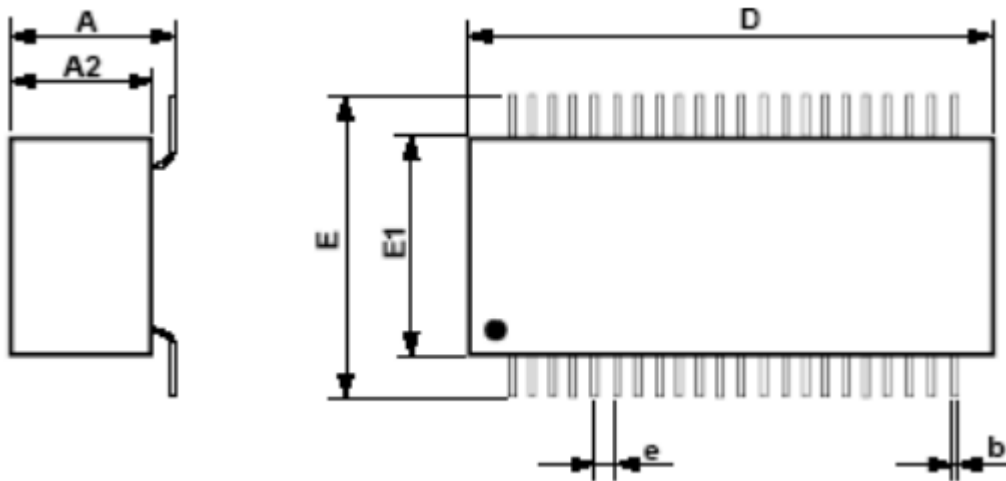


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	4.90	5.60
A2	3.80	4.20
D	23.80	24.20
E	13.40	13.80
E1	10.85	11.05
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	
NOTE : 1. Unit : mm		
2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Mar 24,2018	First Created
A1	May 22, 2018	Modified Operating Temperature Range and Storage temperature.