

# **VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY**

## **VDMR16M08XS54XX4V35 USER MANUAL**

**Version :B1**

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# VDIC-MRAM

## HIGH-SPEED 3.3V 2M×08bit

## MAGNETORESISTIVES RANDOM ACCESS MEMORY

### 1. DESCRIPTION

The VDMR16M08XS54XX4V35 is a 4 x 4,194,304-bit high-speed access time, high-density Magnetoresistives Random Access Memory device. Manufactured with VDIC Very Dense SIP technology, this device stacks 4 4-Mbit MRAM dies. It is organized as four independent dies of 512K x 8bit wide data interface.

The VDMR16M08XS54XX4V35 offers MRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR16M08 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

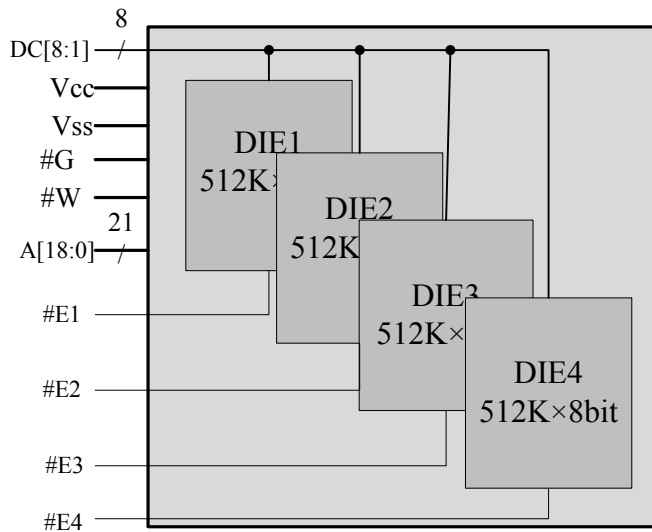
The VDMR16M08XS54XX4V35 has 4 dies. Each die can be selected separately with dedicated #En. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDMR16M08XS54XX4V35 is available in a 54-pin SOP package.

### 2. FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design
- Stack of four 4Mbit MRAM
- Organized as 4 dies of 512K x 8 bit memory
- Four independent Die Select
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- -54-lead SOP package

### 3. BLOCK DIAGRAM



(All other signals are common to five memories)

Figure 1 Block diagram

### 4. PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
NC	1	54	NC
NC	2	53	NC
#E4	3	52	NC
#E3	4	51	NC
#E2	5	50	NC
DC	6	49	DC
NC	7	48	NC
A0	8	47	DC
A1	9	46	A18
A2	10	45	A17
A3	11	44	A16
A4	12	43	A15
#E1	13	42	#G
DQ0	14	41	DQ7
DQ1	15	40	DQ6
VDD	16	39	VSS
VSS	17	38	VDD
DQ2	18	37	DQ5
DQ3	19	36	DQ4
#W	20	35	DC6
A5	21	34	A14
A6	22	33	A13
A7	23	32	A2
A8	24	31	A11
A9	25	30	A10
DC	26	29	DC
DC	27	28	DC

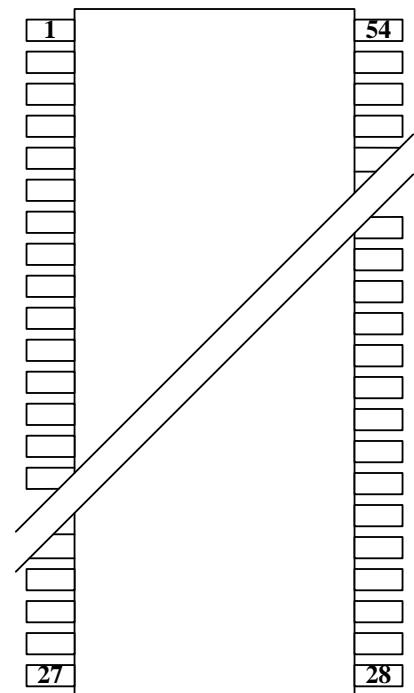


Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#E1	Die select	Disables or enables memory die1 operation
#E2	Die select	Disables or enables memory die2 operation
#E3	Die select	Disables or enables memory die3 operation
#E4	Die select	Disables or enables memory die4 operation
A0 ~ A18	Address	19-bit addresses
#W	Write enable	Enables write operation common to all memory dies
#G	Output enable	Enables data output common to all memory dies
DQ0~ DQ7	Data input/output	Data inputs/outputs 40-bit wide bus
VDD/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	These pins are recommended to be left No Connection on the device.
DC	Do not connect	These pins do not connect

## 5. ELECTRICAL SPECIFICATIONS

### 5.1. ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than the maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on VDD supply relative to Vss	V <sub>DD</sub>	-0.5 ~ +4.0	V
Voltage on any pin relative to Vss	V <sub>IN</sub>	-0.5 ~ V <sub>DD</sub> +0.5	V
Power Dissipation	P <sub>D</sub>	< 1.0	W
Operating Temperature Range	T <sub>OPR</sub>	-55 ~ +95	°C
Storage Temperature Range	T <sub>STG</sub>	-55 ~ +105	°C

## 5.2. RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>	3.0	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>DD</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	-0.5	—	0.8	V
Write inhibit voltage	V <sub>WI</sub>	2.5	2.7	3.0	V

## 5.3. DC ELECTRICAL CHARACTERISTICS

Table 4 DC electrical characteristics

PARAMETERS	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V <sub>OL</sub>	I <sub>OL</sub> = +4mA	—	0.4	V
Output voltage high level	V <sub>OH</sub>	I <sub>OL</sub> = -4mA	2.4	—	V

## 6. TYPICAL APPLICATION

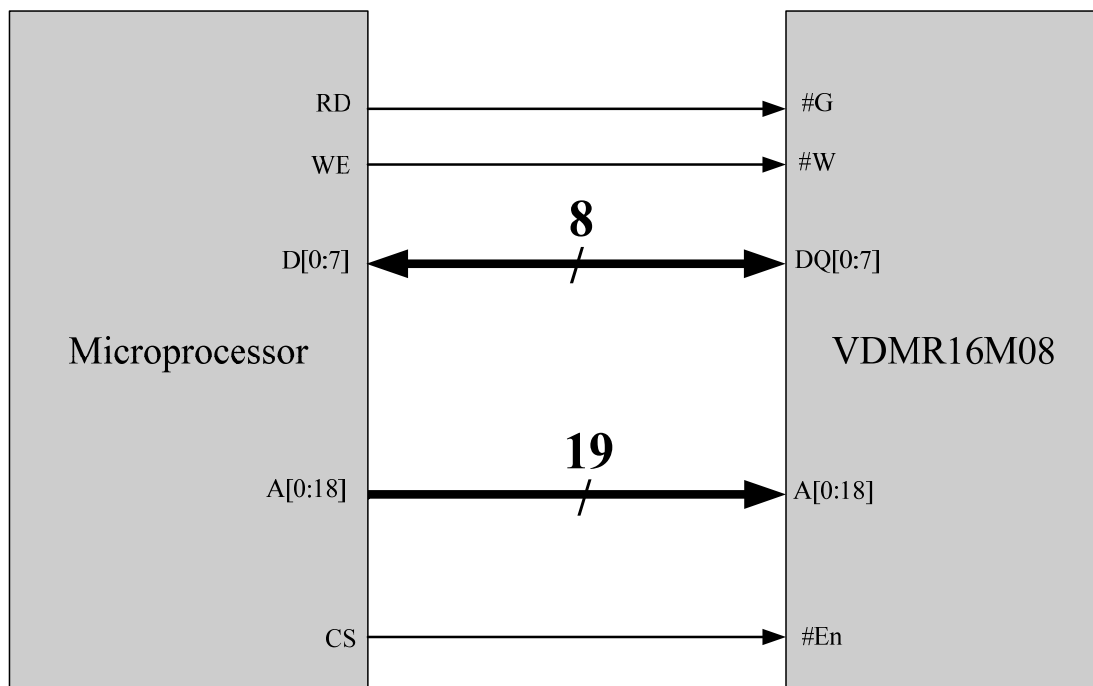


Figure 3 Typical application

## 7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>MR</u>	<u>16M</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>54</u>	<u>X</u>	<u>X</u>	<u>4</u>	<u>V</u>	<u>35</u>	-
VDIC												
MRAM												
Capacity: 16M bit												
Bus Width: 8bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 54 Pin												
Temperature: E=0~+70°C; I=-40~+85°C; S=-55~+95°C												
Quality: E= Sample; B= Industry; S= Space												
Stacking Layer: 4layer												
Power Supply: 3.3V												
Speed: 35ns												
Version: First Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature ( °C )
			TID <sup>1</sup>	SEL <sup>2</sup>	SEU <sup>3</sup>		
VDMR16M08VS54EE4V35	16M	08	-	-	-	SOP54	0 ~ +70
VDMR16M08VS54IB4V35	16M	08	-	-	-	SOP54	-40 ~ +85
VDMR16M08RS54SS4V35	16M	08	TBD	TBD	TBD	SOP54	-55 ~ +95

<sup>1</sup> TID: Total Dose (Krad(Si))

<sup>2</sup> SEL: LET Threshold (Mev.cm<sup>2</sup>/mg)

<sup>3</sup> SEU:SEU Threshold (Mev.cm<sup>2</sup>/mg)

## 8. PACKAGE DIMENSIONS

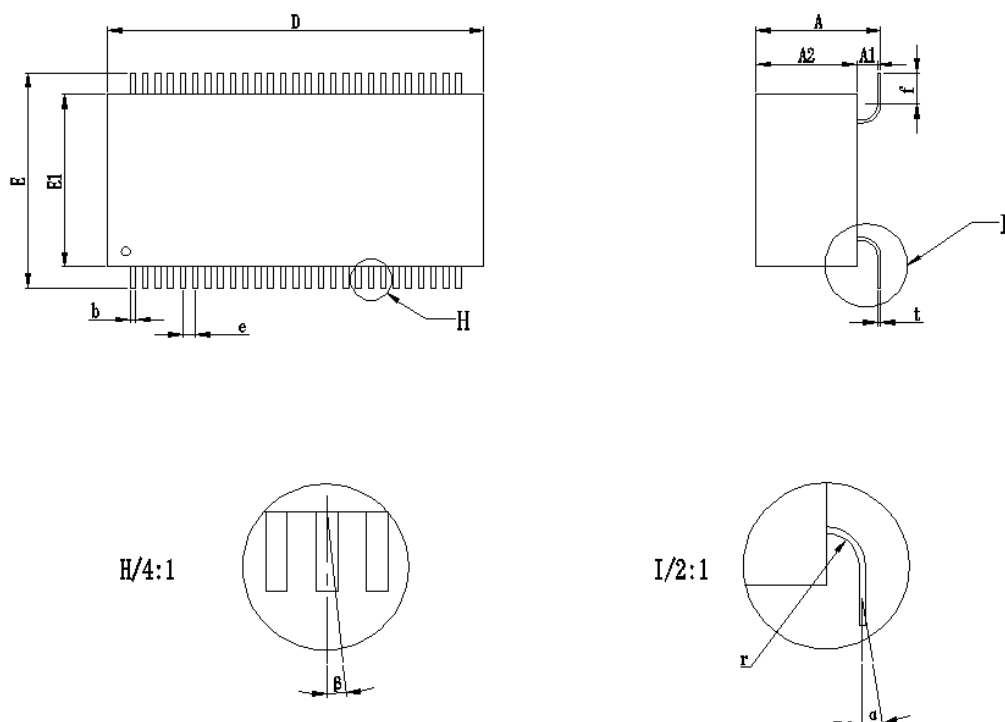


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
$\alpha$	$\leq 3^\circ$	
$\beta$	$\leq 3^\circ$	
NOTE: 1. Unit: mm 2. $A1 = A - A2$		



## 9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Mar 13,2018	Add or reduce the chapters
B0	May 22, 2018	Modified Operating Temperature Range and Storage temperature.
B1	Mar 21,2020	Update TID and SEE