VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD2G72XB134XX5V75 USER MANUAL

Version: A2

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Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 32M×72bit

SYNCHRONOUS DYNAMIC SDRAM

1. DESCRIPTION

The VDSD2G72XB134XX5V75 is a 2,415M bits SDRAM, organized as 32M×72 bits. It is organized with four banks of 512Mbit + Error Checking correction. Each bank has 16-bit interface and is selected with specific #CS, CLK and CKE. It is particularly well suited for use in high reliability, high performance and high density system applications, such as solid state mass recorder server or workstation.

The VDSD2G72XB134XX5V75 is packaged in a 134 ball BGA.

2. FEATURES

- Stack of five 512Mbit SDRAM.
- Organized as 32M×72 bit.
- Single +3.3V±0.3V power supply.
- Fully synchronous; all signals registered on positive edge of system clock.
- Internal pipelined operation; column address can be changed every clock cycle.
- Programmable burst lengths: 1, 2, 4, 8 or full page.
- Auto Precharge, includes Concurrent Auto Precharge, and Auto Refresh Modes.
- Self-Refresh Modes.
- LVTTL-compatible inputs and outputs.
- Available Temperature Range :

  0℃ to +70℃.

  -40℃ to +85℃.

  -55℃ to +105℃.

3. BLOCK DIAGRAM

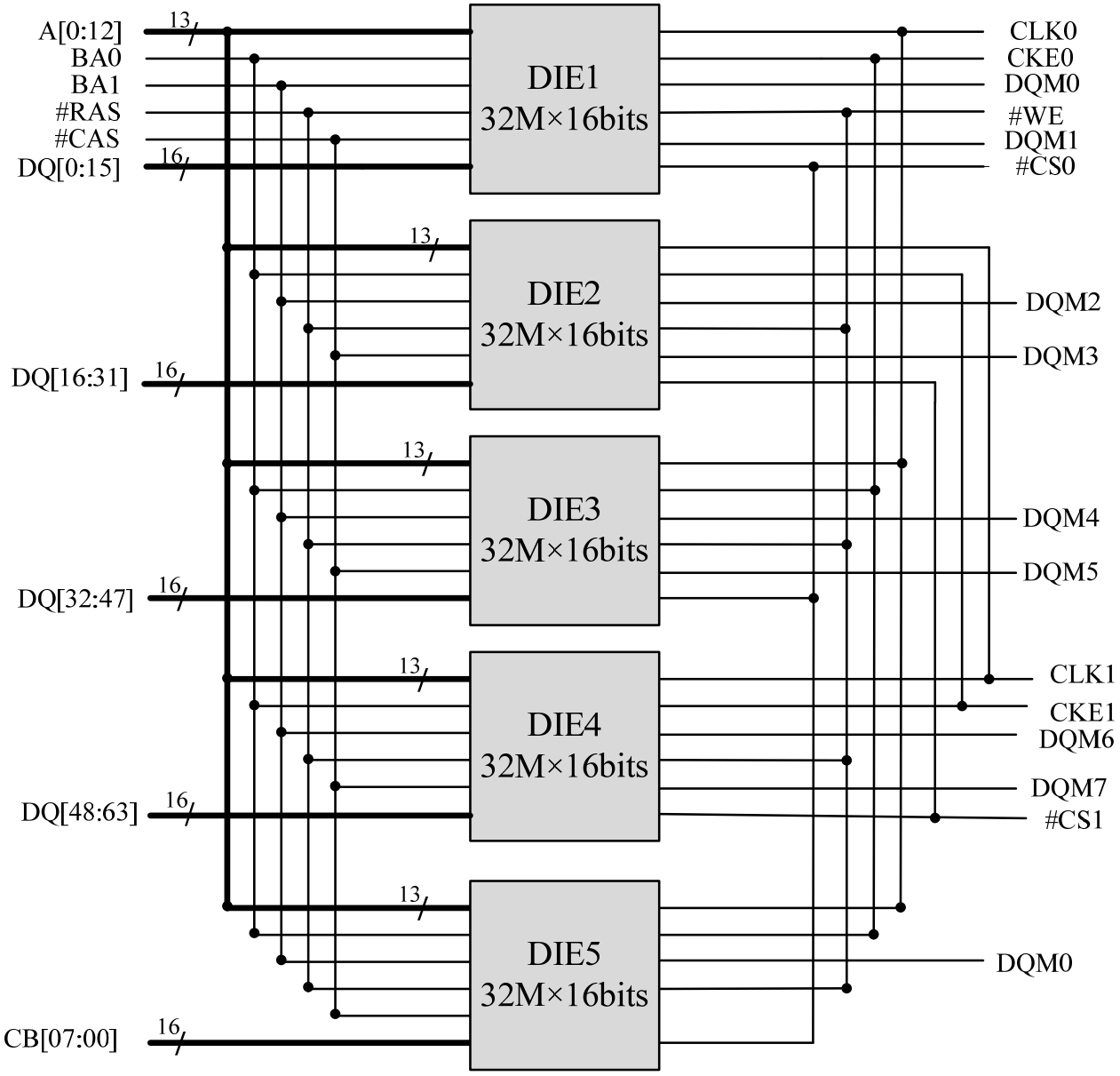

Figure 1 Block Diagram

4. PIN DESCRIPTIONS

Pin ID	Pin NO.			Pin Id	Pin ID	Pin NO.			Pin ID	Pin ID	Pin NO.
	A1		D1	DQ18	DQ6	G1		K1	#CS1	A2	N1
DQ33	A2		D2	DQ2	DQ22	G2		K2	#CS0	VDD	N2
DQ49	A3		D3	DQ17	VSS	G3		K3	#RAS	DQ53	N3
VDD	A4		D4	DQ16	DQM1	G4		K4	NC	DQ52	N4
VSS	A5		D5	DQ61	VDD	G5		K5	VSS	DQ59	N5
DQ62	A6		D6	CB04	DQ25	G6		K6	CKE1	DQ40	N6
DQ47	A7		D7	DQ31	DQ9	G7		K7	CKE0	CB01	N7
CB05	A8		D8	DQ13	DQ10	G8		K8	NC	VSS	N8
VSS	A9		D9	VDD	DQ26	G9		K9	NC	A5	N9
DQ0	B1		E1	DQ19	DQ7	H1		L1	BA0	VDD	P1
DQ48	B2		E2	DQ3	DQ23	H2		L2	NC	DQ55	P2
DQ34	B3		E3	VSS	VDD	H3		L3	BA1	DQ37	P3
DQ35	B4		E4	DQ4	DQM3	H4		L4	A10	DQ36	P4
DQ44	B5		E5	DQ45	DQ8	H5		L5	VSS	DQ43	P5
DQ46	B6		E6	VSS	VSS	H6		L6	A6	DQ41	P6
CB06	B7		E7	DQ30	VSS	H7		L7	A9	CB02	P7
DQ15	B8		E8	DQ29	DQM0	H8		L8	A11	VSS	P8
VSS	B9		E9	DQ11	DQM2	H9		L9	A12	VSS	P9
DQ01	C1		F1	VDD	#CAS	J1		M1	A0	VDD	R1
DQ32	C2		F2	DQ20	#WE	J2		M2	A1	DQ38	R2
DQ50	C3		F3	DQ5	DQM7	J3		M3	A3	DQ54	R3
DQ51	C4		F4	DQ21	DQM5	J4		M4	DQ39	VDD	R4
DQ60	C5		F5	VSS	DQ24	J5		M5	DQ58	VSS	R5
DQ63	C6		F6	DQ12	DQM4	J6		M6	DQ42	DQ57	R6
CB07	C7		F7	DQ28	DQM6	J7		M7	A4	DQ56	R7
DQ14	C8		F8	DQ27	CLK1	J8		M8	A7	CB03	R8
VDD	C9		F9	VSS	CLK0	J9		M9	A8	CB00	R9

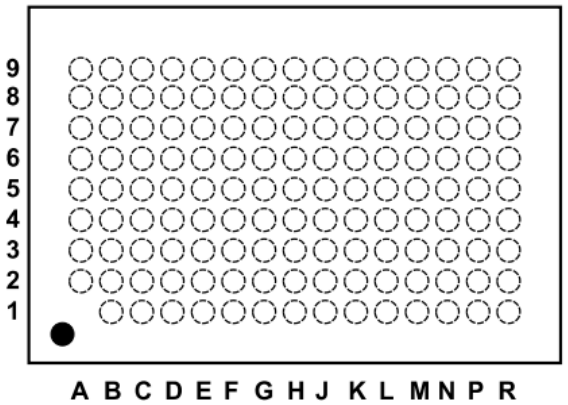

Figure 2 Pin Configuration

Table 1 Pin Description

Name	Description
A0~A12	Row Address Input
A0~A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ63, CB00 to CB07	Data I/O
CLK	System Clock Input
CKE	Clock Enable
#CS0 to #CS1	Chip Select
#RAS	Row Address Strobe Command
#CAS	Column Address Strobe Command
#WE	Write Enable
DQM0 to DQM7	Input/Output Mask
VDD	Power
VSS	Ground
NC	No Connection

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{DD}	-0.5 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ V_{DD}+0.5	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 ~ +105	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
	V_{IL}	-0.3	——	0.8	V

5.3 DC Electrical Characteristics

Table 4 DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	V_{DD}=3.0V, I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	V_{DD}=3.6V, I_{OL}=2mA	——	0.4	V

6. TYPICAL APPLICATION

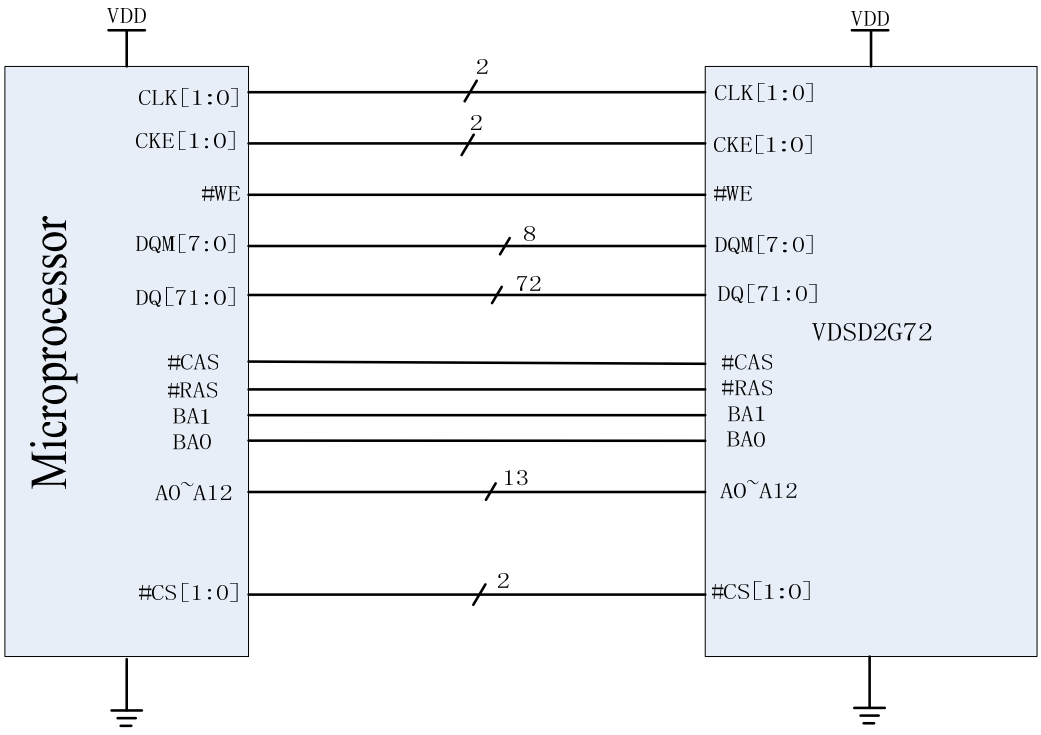

Figure 3 Typical Application

7. ORDERING INFORMATION

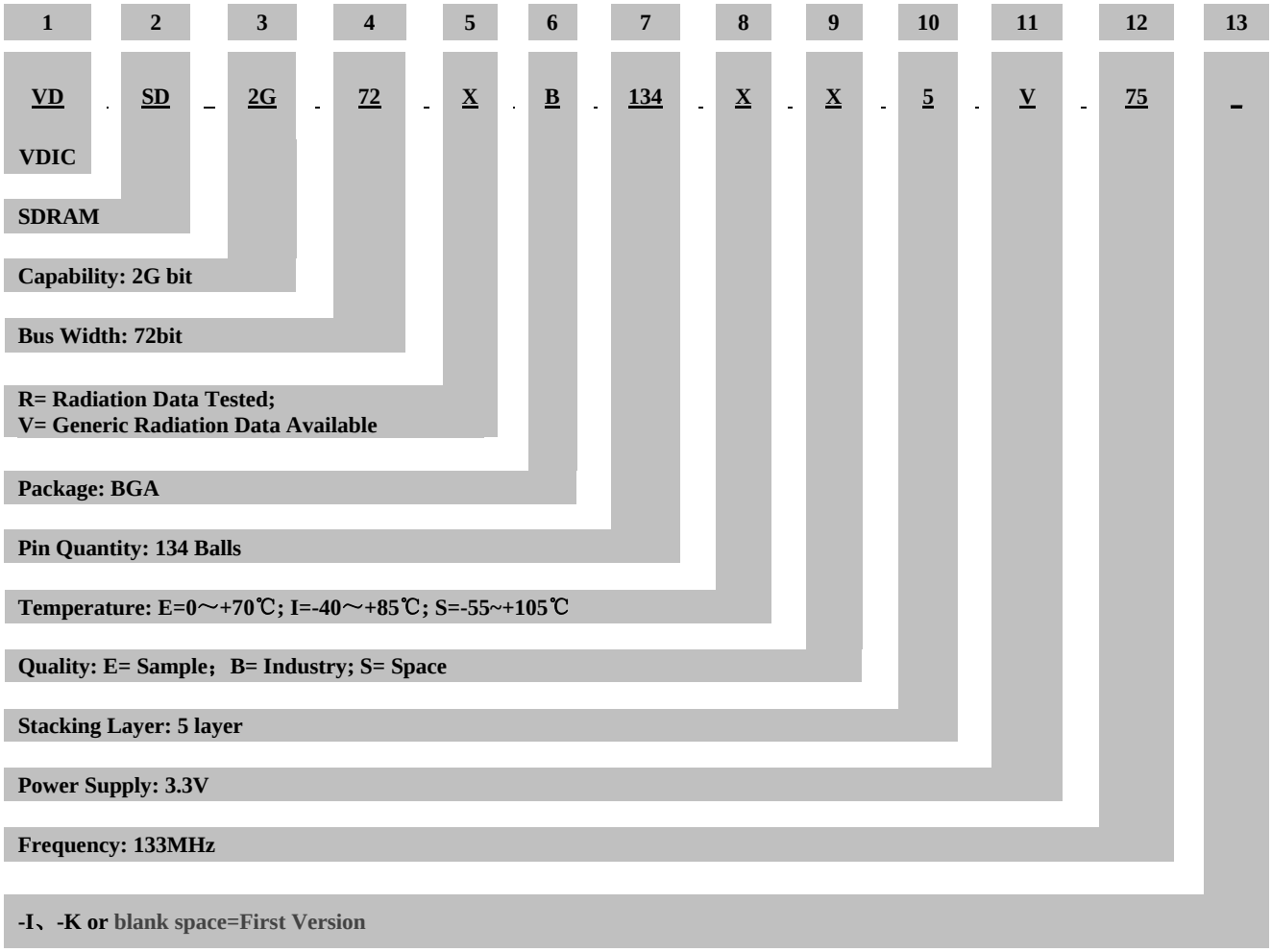

Table 5 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD2G72VB134EE5V75	2G	72	-	-	-	BGA134	0 ~ +70
VDSD2G72VB134IB5V75	2G	72	-	-	-	BGA134	-40 ~ +85
VDSD2G72RB134SS5V75	2G	72	>50	>80	1	BGA134	-55 ~ +105

[1] TID: Total Dose (Krads(Si))
[2] SEL: LET Threshold(Mev.cm^2/mg)
[3] SEU:SEU Threshold (Mev.cm^2/mg)

8. PACKAGE DIMENSIONS

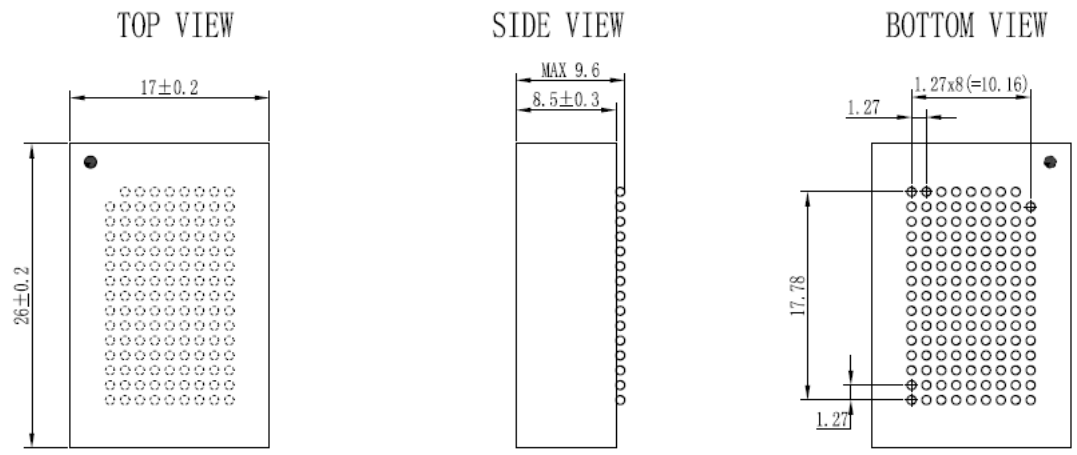

Figure 4 Package dimensions

9. REVISION HISTORY

Table 6 Revision History

Revision	Date	Description of Change
A0	Oct 17, 2018	Initial Release
A1	Mar 19, 2020	Update text format
A2	Jun 17, 2021	Update description and features