VDIC ASYNCHRONOUS STATIC RAM

VDSR20M40XS84XX2V12 USER MANUAL

Version : A1

Document NO.: ORBITA/SIP-VDSR20M40XS84XX2V12-USM-01
Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park，NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai，*Guangdong,* China 519080
Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

VDIC-SRAM

HIGH-SPEED 512K x 40bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR20M40XS84XX2V12 is a high-speed access time, high-density Static Random Access Memory with 20Mbit. Manufactured with VDIC—Very Dense SIP technology, this die stacks six SRAM dies employing CMOS process (6-transistor memory cell). It is organized as two 256 x 40bit banks, each bank has 2 group of chip select signals #CS and #WE to control the 32bit and 8bit independently.

Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR20M40XS84XX2V12 is available in a 84-pin SOP package.

2 Features

- Single 3.3V± 0.3V power supply
- Six Dies with four independent Selects: #CS0、#CS1、#CS2、#CS3
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Access time: 12ns
- No clock or timing strobe required
- 84-lead SOP Type II package

3 Block Diagram

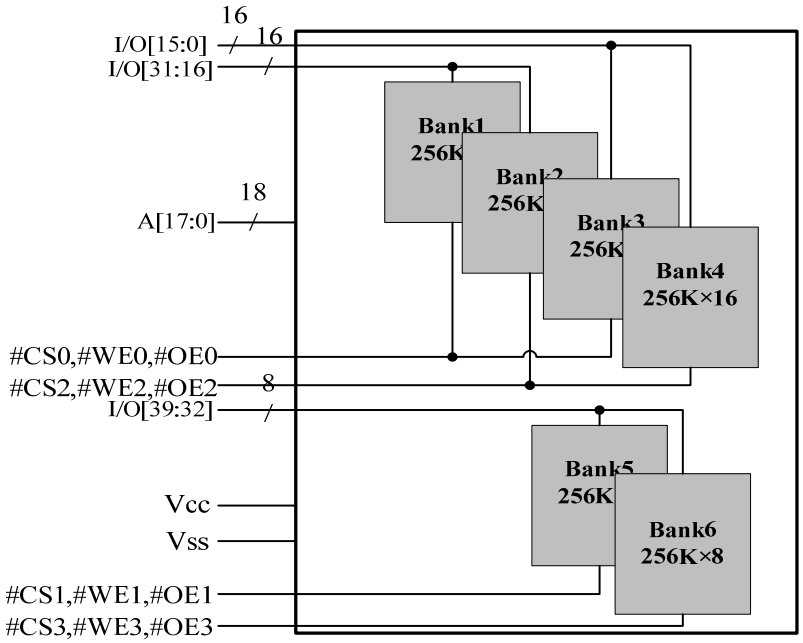


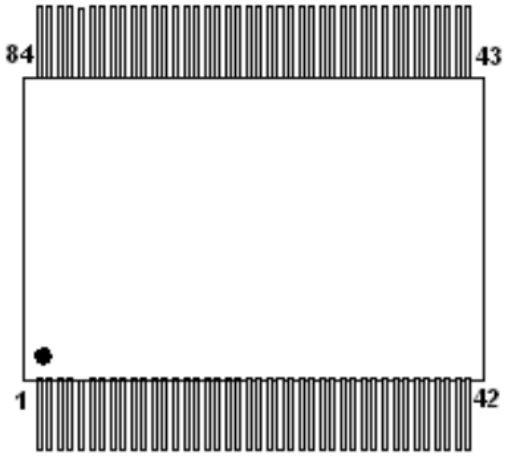
Figure 1: Block diagram

4 Pin Descriptions

Pin Id	Pin#		Pin Id	Pin Id	Pin#		Pin Id
I/O0	1	22	VSS	#WE3	43	64	VSS
I/O1	2	23	I/O20	#WE1	44	65	I/O28
I/O2	3	24	I/O21	#OE3	45	66	I/O29
I/O3	4	25	I/O22	#OE1	46	67	I/O30
VCC	5	26	I/O23	VCC	47	68	I/O31
VSS	6	27	A4	VSS	48	69	A16
I/O4	7	28	A5	#CS3	49	70	A17
I/O5	8	29	A6	#CS1	50	71	#WE2
I/O6	9	30	VSS	A9	51	72	#WE0
I/O7	10	31	A7	A10	52	73	#OE2
#CS0	11	32	A8	A11	53	74	#OE0
#CS2	12	33	I/O32	A12	54	75	I/O8
A0	13	34	I/O33	VSS	55	76	I/O9
A1	14	35	I/O34	A13	56	77	I/O10
A2	15	36	I/O35	A14	57	78	I/O11
A3	16	37	VCC	A15	58	79	VCC
I/O16	17	38	VSS	I/O24	59	80	VSS
I/O17	18	39	I/O36	I/O25	60	81	I/O12
I/O18	19	40	I/O37	I/O26	61	82	I/O13
I/O19	20	41	I/O38	I/O27	62	83	I/O14
VCC	21	42	I/O39	VCC	63	84	I/O15

Figure 1 Pin configuration

Table 1 Pin description



Pin	Name	Function
#CS0	Die select	Disables or enables memory bank1 and bank3 operation
#CS1	Die select	Disables or enables memory bank 5 operation
#CS2	Die select	Disables or enables memory bank 2 and bank 4 operation
#CS3	Die select	Disables or enables memory bank 6 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all memory banks
#OE	Output enable	Enables data output command to all memory banks
I/O0~ I/O39	Data input/output	Data inputs/outputs 40-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to +V_{CC}+0.5	V
Power Dissipation	P_D	3.0	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{CC}+0.5	V
Input low voltage	V_{IL}	-0.5	——	0.8	V

5.3 DC Electrical Characteristics

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V, I_{OL}=1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-0.5mA	2.4	——	V

6 Typical Application

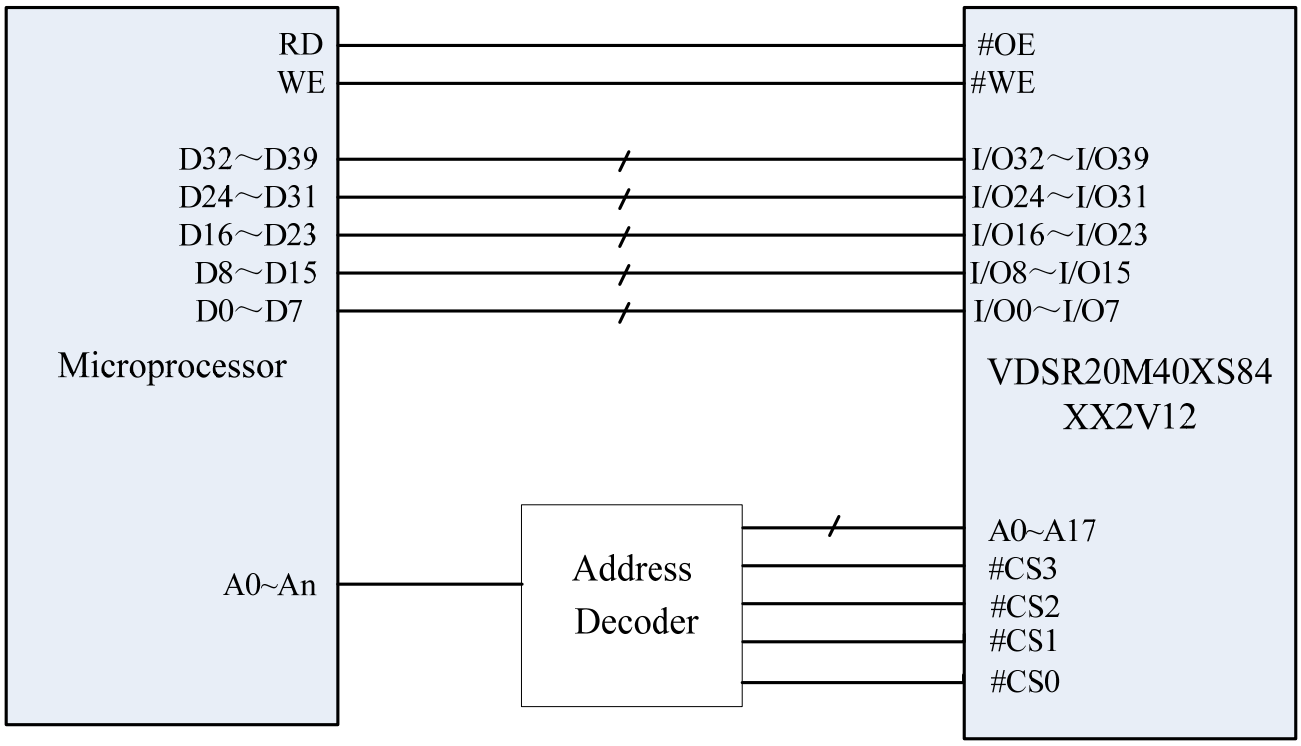


Figure 2 Typical application

7 Ordering Information

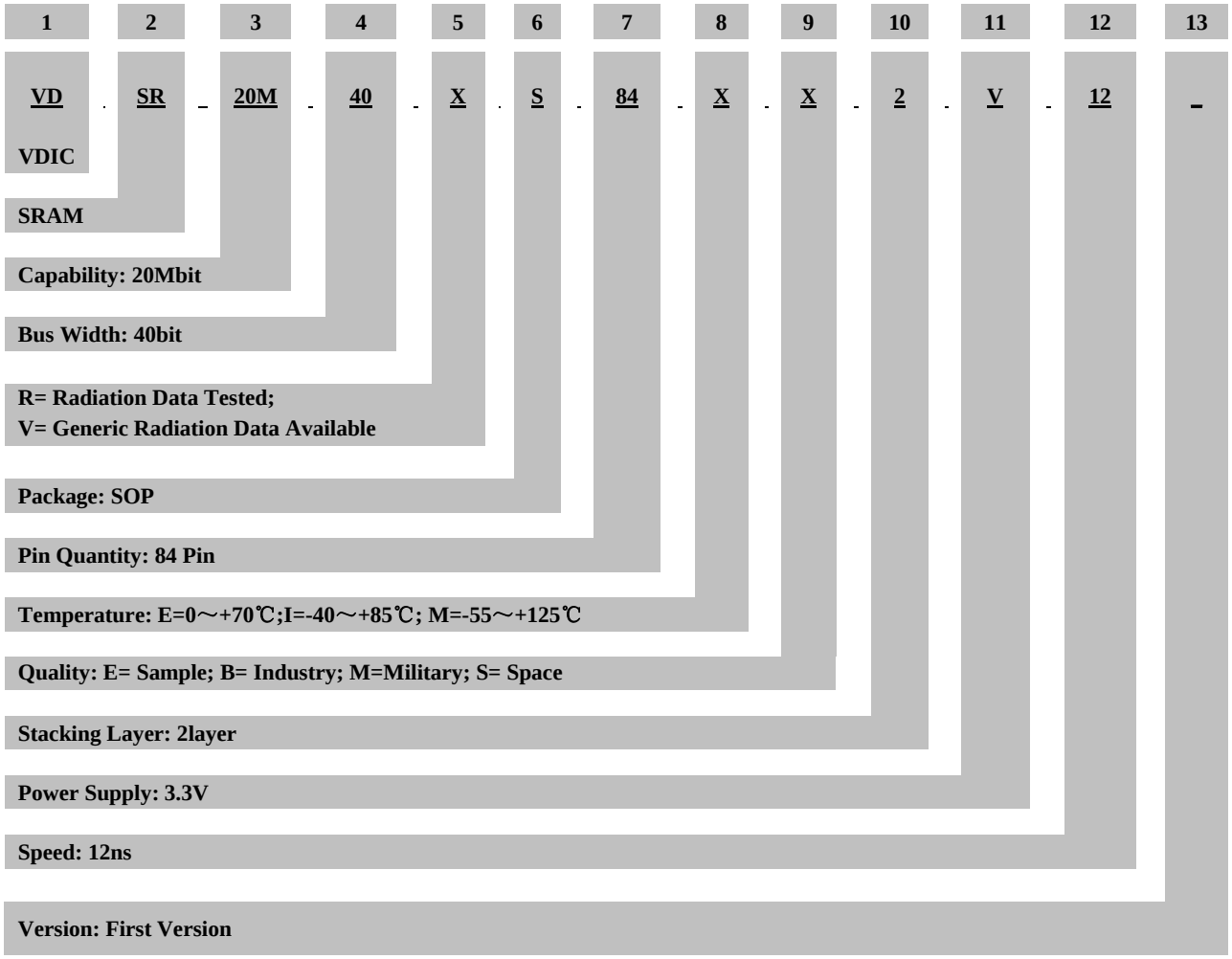


Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR20M40VS84EE2V12	20M	40	-	-	-	SOP84	0 ~ + 70
VDSR20M40VS84IB2V12	20M	40	-	-	-	SOP84	-40 ~ + 85
VDSR20M40VS84MM2V12	20M	40	-	-	-	SOP84	-55 ~ + 125
VDSR20M40RS84MS2V12	20M	40	> 100	> 75	> 0.9	SOP84	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 Package Dimensions

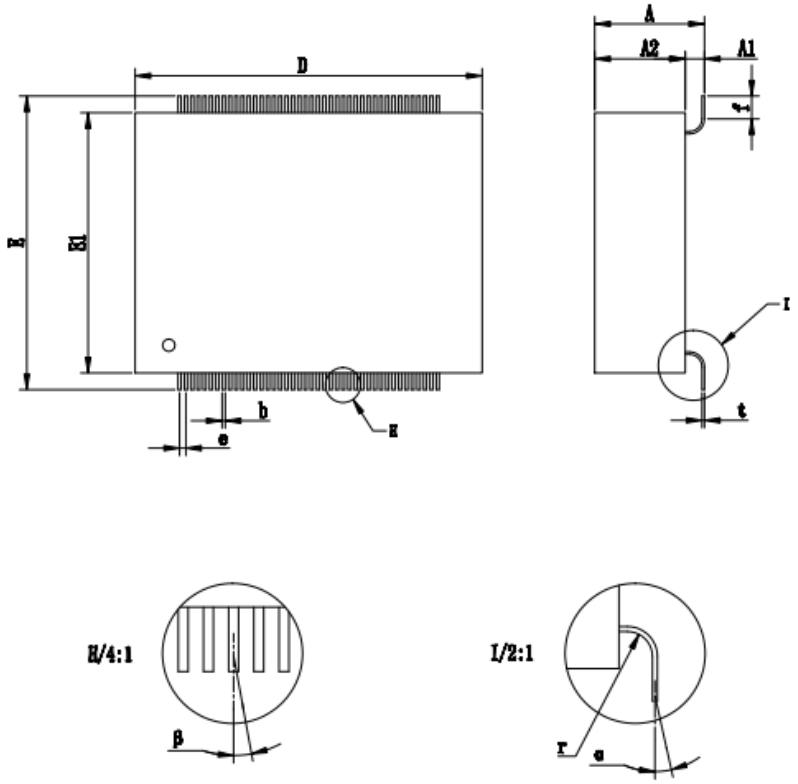


Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	8.30	9.00
A2	7.10	7.70
D	27.80	28.20
E	23.50	23.90
E1	20.80	21.20
f.	1.80	
b	0.25	
e	0.508	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9 Revision History

Table 7 Revision history

Revision	Date	Description of Change
A0	May 27,2019	First Created
A1	Mar 21,2020	Update TID and SEE